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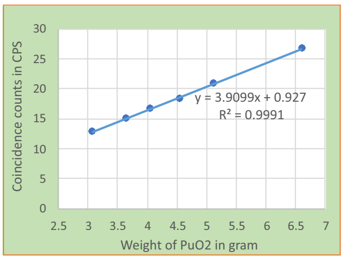
एनडब्ल्यूसीसी प्रणाली हेतु एक स्वदेशी एफपीजीए-आधारित संपात गणना मॉड्यूल का विकास

शुभम कावडे[1], एस.बी. म्हात्रे[1], ए. पांडेय[1], पियुष पुरोहित[1], अनूप केल्कर[1], डी.बी. साठे[1], सौरभ मोइत्रा[2], नीलिमा कांबले[2], प्रफुल्ल सतीश[2] और संजू जॉय[2]

[1]ईंधन संविरचन प्रभाग, नाभिकीय पुनःचक्रण बोर्ड, भाभा परमाणु अनुसंधान केंद्र, तारापुर-401502, भारत
[2]इलेक्ट्रॉनिकी प्रभाग, भाभा परमाणु अनुसंधान केंद्र, ट्रांबे, मुंबई-400085, भारत



सीपीएस बनाम PuO_2 Wt. में संयोग की गणना । (एफपीजीए आधारित)

सारांश

$(U, Pu)O_2$ मिश्रित ऑक्साइड (MOX) मिश्रित पाउडर में, प्लूटोनियम की मात्रा का निर्धारण न्यूट्रॉन वेल कोइनसिडेन्स काउंटर (एनडब्ल्यूसीसी) तकनीक का उपयोग करके प्रक्रम नियंत्रण विधियों द्वारा किया जाता है। मौजूदा प्रणाली ने पारंपरिक इलेक्ट्रॉनिक्स को नियोजित किया, जो रखरखाव और संगतता में सीमा संतुलन बनाता है। चूंकि ऐसी प्रणालियाँ निर्यात नियंत्रण के तहत प्रतिबंधित हैं और भारत में व्यावसायिक रूप से अनुपलब्ध हैं, इसलिए विभाग की निष्क्रिय न्यूट्रॉन आमापन गतिविधियों को समर्थ बनाने के लिए स्वदेशी विकास अत्यंत आवश्यक है। इसे प्राप्त करने के लिए, भापअ केंद्र, मुंबई में इलेक्ट्रॉनिक्स प्रभाग ने एक स्व-स्थाने फील्ड प्रोग्रामेबल गेट ऐरे (एफपीजीए) आधारित संयोग मॉड्यूल विकसित किया। इसमें संबद्ध सिग्नल प्रक्रम इलेक्ट्रॉनिकी एवं डाटा अधिप्राप्ति, चाक्षुषीकरण एवं पैरामीटर विन्यास के लिए एक ग्राफिकल यूज़र इंटरफेस है, जो एफएफ, आईएनआरपी(ओ), तारापुर में समान परिस्थितियों के तहत पारंपरिक प्रणाली के साथ-साथ भावी अनुसंधान हेतु अग्रसर करता है, मॉड्यूल ने बेहतर स्थिरता और गणना की सटीकता का प्रदर्शन करते हुए, 0.997 से 0.999 तक सहसंबंध मान(R^2) प्राप्त किया। यह कार्य निरंतर न्यूट्रॉन संयोग माप के लिए जारी रखे जाने योग्य, पूर्णत: स्वदेशी समाधान प्रदान करता है।

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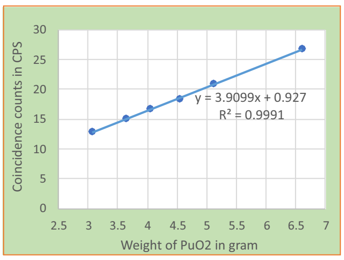
Development of an Indigenous FPGA-Based Coincidence Counting Module for NWCC System

Shubham Kawde[1]*, S. B. Mhatre[1], A. Pandey[1], Piyush Purohit[1], Anoop Kelkar[1], D. B. Sathe[1]
Sourabh Moitra[2], Neelima Kamble[2], Prafulla Satish[2] and Saju Joy[2]

[1]Fuel Fabrication Division, Nuclear Recycle Board, Bhabha Atomic Research Centre, Tarapur-401502, INDIA
[2]Electronics Division, Bhabha Atomic Research Centre, Trombay, Mumbai-400085, INDIA



Coincidence counts in CPS Vs PuO_2 Wt.(FPGA Based)

ABSTRACT

In (U, Pu) O Mixed Oxide (MOX) blended powder, plutonium content is determined by process control methods using the Neutron Well Coincidence Counter (NWCC) technique. The existing system employed legacy electronics, posing limitations in maintainability and compatibility. Because such systems are restricted under export controls and commercially unavailable in India, indigenous development is absolutely essential to support the Department passive neutron assay activities. To address this, the Electronics Division at BARC, Mumbai, developed an in-house Field Programmable Gate Array (FPGA) based coincidence module. It features associated signal processing electronics and a graphical user interface for data acquisition, visualization, and parameter configuration, enhancing flexibility for future research. Tested alongside the legacy system under identical conditions at F.F., INRP(O), Tarapur, the module demonstrated improved stability and counting accuracy, achieving correlation values (R^2) from 0.997 to 0.999. This work provides a maintainable, fully indigenous solution for sustained neutron coincidence measurements.

KEYWORDS: *FPGA, Gate Array, NWCC, Neutron Well, Coincidence Counter, Electronics, HDPE, Software, IC, Module*

**Author for Correspondence: Shubham Kawde*
E-mail: skawde@barc.gov.in

Introduction

Quantitive analysis of Plutonium is an essential task in MOX fuel fabrication. Passive neutron coincidence counting is a well-established nondestructive assay technique used for estimating plutonium content in MOX fuel fabrication and safeguards applications [1]. Conventional chemical analysis methods, although precise, are slow, require elaborate sampling procedures, and generate α-active liquid waste, making them unsuitable for routine large scale operations. Earlier studies at BARC have demonstrated that NWCC, provide fast, reliable, and waste-free verification of PuO enrichment in MOX fuel blends as well as in recycled materials such as Clean Rejected Oxide (CRO) powder and Dirty Rejected Oxide (DRO) powder [2]. NWCC distinguishes spontaneous fission neutrons from random (α,n) neutrons by analysing their time correlation. In plutonium-bearing MOX powders, spontaneous fission from even-even isotopes (mainly ^{238}Pu, ^{240}Pu, ^{242}Pu) provides correlated events, while (α,n) neutrons from oxygen contribute an uncorrelated background [1]. Earlier work at BARC Tarapur established NWCC as a practical tool for verifying PuO content across a wide range of sample sizes and demonstrated strong agreement with chemical methods for MOX pellets [2]. For detect coincidence event, different types of coincidence detection circuits have been described by Ensslin et al., who demonstrated that shift-register-based systems significantly reduce system dead time [1]. NWCC systems subsequently relied on shift-register-based electronics, first conceptualized by Boehnel et al. [1,3]. The electronic circuitry was further developed by Stephens et al. [4] and later improved by Swansen et al. [5,6] and Lambert et al. [7]. The shift-register concept enabled a substantial reduction in coincidence dead time and allowed measurements at higher count rates.

The design by Swansen et al. provided selectable gate widths (8-128 μs) and pre-delays (1-32 μs), enabling reliable operation at total count rates of several hundred kHz. Similar systems were also developed and optimized at BARC by S. P. Dange et al. and S. C. Kapoor et al., incorporating a fixed 8 μs delay and two selectable gate widths of 64 μs and 128 μs [8,9]. However, these systems were implemented using discrete electronic components, many of which are now obsolete and no longer commercially available, creating challenges for long-term maintenance and reproducibility. In addition, the available gate widths were restricted to discrete values that are multiples of 2^n, limiting optimization for different detector geometries and measurement conditions. Furthermore, the Real + Accidental (R + A) and Accidental (A) outputs obtained from the scalers do not represent true event counts, as the circuitry generates a single TTL pulse only when the accumulator exceeds a fixed threshold of ten counts.

To overcome these limitations, an FPGA-based coincidence counting module with associated signal-processing electronics was developed in-house at Electronics Division, BARC. The system was tested in parallel with the existing setup at F.F., INRP(O), Tarapur, under identical conditions. The developed system provides a flexible and maintainable indigenous solution compatible with established NWCC practices and can be extended for applications such as multiplicity counting and safeguards.

Overview of Existing System

The current system installed at F.F., INRP(O) was developed by the Radiochemistry Division, BARC, Mumbai, in 1993. The development and optimization details of this system are described in [8,9]. The block diagram of the system is shown in Figure 1. The system consists of the following units:

Detector Assembly: It is made up of 16 He-3 counters (50 cm length; 2.54 cm diameter and filled with He-3 at 4 Atm. pressure) arranged in single concentric array within the moderator housing of High-Density Polyethylene (HDPE).

Pre Amplifier: A single charge-sensitive preamplifier has been used for both high voltage biasing and amplification of the signal received from the detector assembly.

Amplifier: A single width Nuclear Instrumentation Module (NIM) Spectroscopy amplifier having variable gain (1 to 1000).

Coincidence Unit: The coincidence unit is a double width NIM module based on shift-register logic for neutron coincidence counting. Input pulses from the amplifier are discriminated into standard logic pulses and synchronized with the system clock for processing. A fix pre-delay is introduced using an 8-bit shift register to accommodate detector and amplifier recovery time and to avoid bias between the real-plus-accidental (R+A) and accidental (ACC) gates. The prompt R+A gate is implemented using a 64-bit shift register, providing selectable gate widths of 64 μs or 128 μs. Coincidence events within the R+A and ACC gates are continuously monitored using an up-down counter, which tracks the number of pulses present in the gate at any instant.

The counter output is processed through binary adders, converted to BCD format using binary-to-BCD converters, and accumulated in register latches. A fixed long delay of 1024 μs between R+A and ACC sampling is generated using cascaded 64-bit shift registers. Each input pulse independently generates its own R+A and ACC sampling gates, eliminating the need to wait for gate closure and resulting in very low system dead time. This architecture allows operation at counting rates of several kilohertz. An underflow detection circuit provides fault indication, while the accumulated R+A and ACC counts are displayed using LED-based readouts.

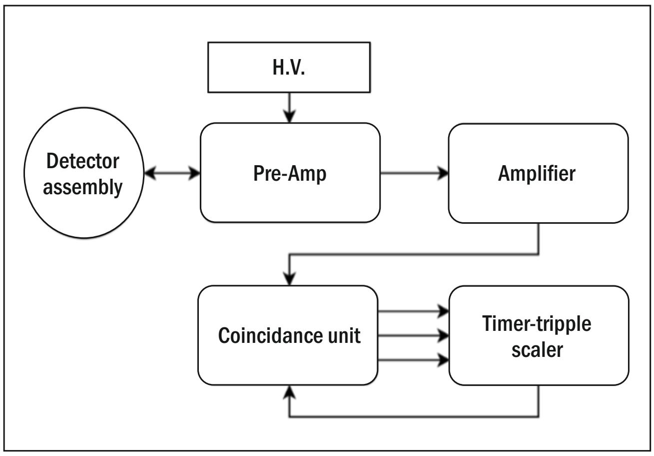


Fig.1: Block diagram of NWCC system.

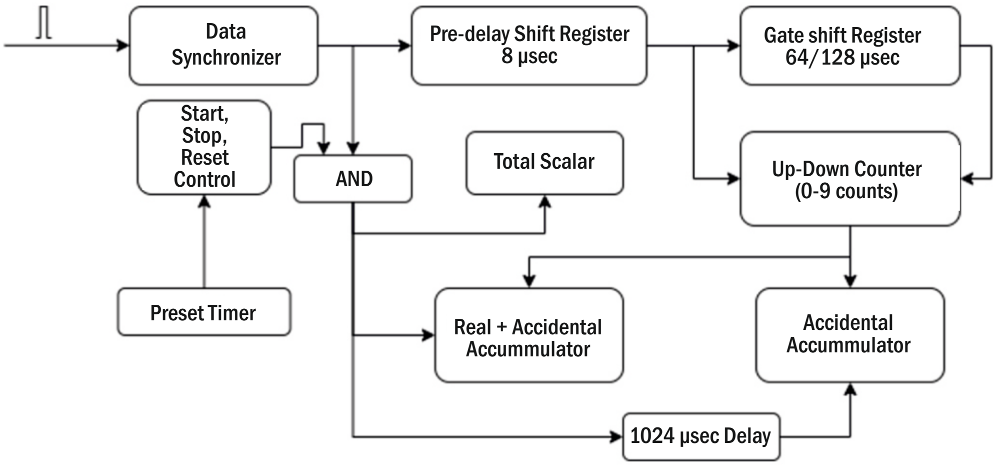


Fig.2: Block diagram of coincidence counter.

Details of FPGA based NWCC System

Electronics Division, BARC, had undertaken the development of the new portable and compact NWCC system based on the requirements of Fuel Fabrication Division, Nuclear Recycle Board, BARC, Tarapur and have delivered two NWCC units along with associated low noise charge sensitive pre-amplifiers (CSPA) for the He-3 Neutron well detector assembly.

One complete NWCC system consists of HDPE well with 16 detector assembly, CSPA (mounted very close to the detector assembly) and a compact and portable (25 cm X 30 cm X 15 cm) NWCC module comprising a variable HV supply, a variable gain spectroscopy amplifier, a discriminator logic, CSPA supply for external CSPA. A 1.5 KV, 1.3 mA HV supply is used for biasing multiple He-3 detectors in the detector assembly with a FPGA based programmable HV control logic with a voltage setting resolution of 1V in 1500V, a high count rate (maximum 200K CPS) FPGA based coincidence counter, and an Ethernet interface for data exchange with the command and control PC running the NWCC analysis software. The new NWCC system being portable and operating on 230V AC mains mitigates the need for large and heavy specialized supply bins used with the earlier NIM based NWCC system.

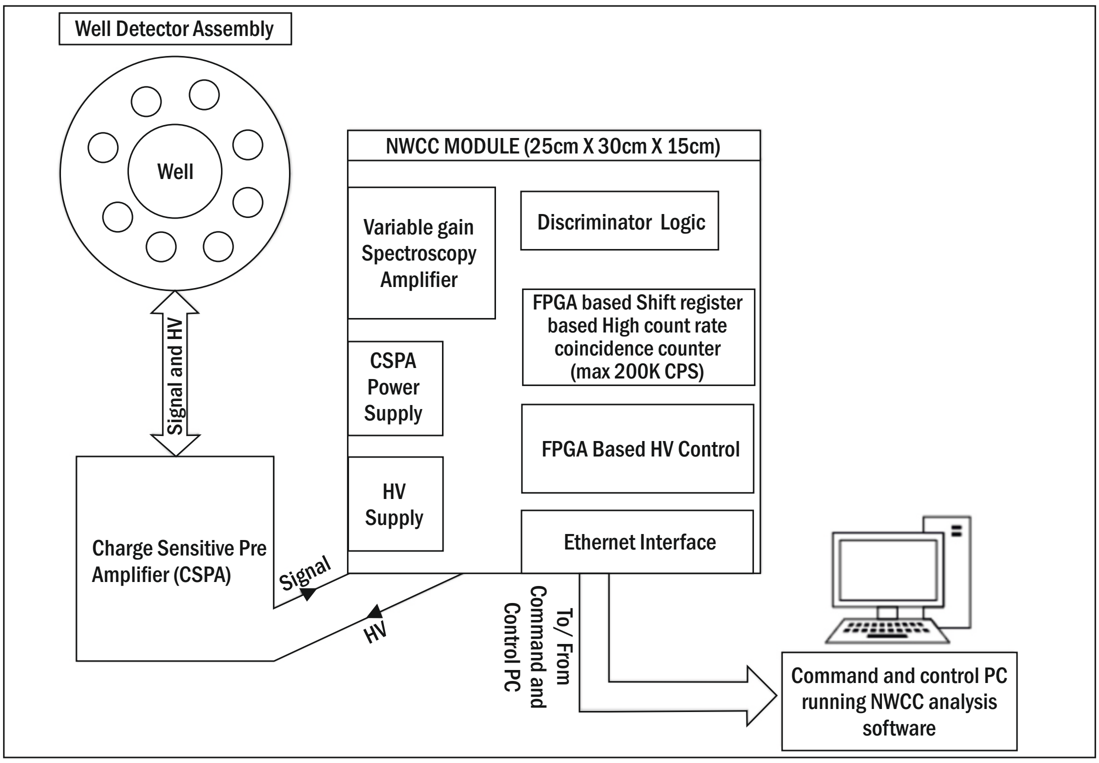


Fig.3: Block Diagram of the complete FPGA based NWCC System.

The technical specifications of the various electronic sub-modules of the NWCC system are as follows.

(A) Charge Sensitive Pre Amplifier (CSPA):

(a) **Charge Sensitivity (Si equivalent):** Nominally 45 mV/MeV.

(b) **Rise Time:** < 10 ns at 0 pF

(c) **Input:** Accepts positive or negative charge input from detector.

(d) **Bias:** Accepts detector bias from bias supply generated at NWCC module and applies it to detector through the input connector, maximum ±1500 V, 1.3 mA

(e) **Power:** Input power through 2-meter power cable from 9 pin D type connector in shaping amplifier in the NWCC module.

(B) Spectroscopy Amplifier:

(a) **Gain Range:** Continuously adjustable from 10 to 500.

(b) **Pulse Shape:** Unipolar Gaussian pulse shape at the output.

(c) **Shaping Time:** 1 μsec (Fixed).

(C) Discriminator Logic:

(a) **Lower Level Discriminator (LLD):** Variable LLD level from 0V to 6V settable with a voltage setting resolution of 50 mV in the range.

(b) **Upper Level Discriminator (ULD):** Variable ULD level from 0V to 10V settable with a voltage setting resolution of 50 mV in the range.

(D) Programmable High Voltage:

(a) **Output Range:** 0 V to 1500 V with a voltage setting resolution on 1V (controlled by PC over Ethernet via FPGA based HV control algorithm)

(b) **Maximum Current range:** 1.3 mA.

(c) **Interface:** Connected to the Pre-amplifier via a 1-meter long Safe High Voltage (SHV) cable.

(E) FPGA based Coincidence Counter: The coincidence logic has been implemented in the FPGA through HDL based firmware development, following the coincidence algorithm described in [3]. Since the logic is realized using HDL, all operational parameters (Pre-delay, gate width, long delay) and functional features of the coincidence system are fully configurable and can be adapted for various passive neutron assay applications within the department with only minor modifications to the firmware. For the INRP(O) system, which employs 16, He-3 detectors arranged in a well-type geometry, the coincidence logic has been configured with the following parameters:

(a) **Pre-Delay:** Variable pre-delay time settable from 1 μsec to 32 μsec with a setting resolution of 1 μsec.

(b) **Gate Width:** Variable gate width settable from 8 μsec to 128 μsec with a setting resolution of 8 μsec (i.e. 8, 16, 24, 32 ....112, 120, 128).

(c) **Maximum Count Rate:** 200K counts per second.

(F) NWCC Analysis Software (Running on PC):

(a) The software provides command and control GUI on a PC for data acquisition from NWCC system hardware and for setting various hardware parameters over Ethernet.

(b) The software also allows the user to automate preprogrammed acquisition runs for a preprogrammed duration using the automation module in the software.

(c) The software can also generate regression plots from the data acquired from multiple samples and can compute the R^2 value.

Experiment and Results

To validate the performance of the FPGA based Coincidence Counting Module, an experimental setup was configured. A single preamplifier and spectroscopy amplifier was used to ensure identical input signal conditions for both coincidence counting units under comparison. The output of the spectroscopy amplifier was split into two identical signal paths. Each path was fed simultaneously to the FPGA based coincidence module and the reference coincidence module.

Identical operating parameters were configured in both coincidence modules:

- **Pre-delay:** 8 μs
- **Gate width:** 128 μs
- **Threshold:** 2.5 V

A standard PuO source was used for testing. The mass of the PuO source ranged from 3 g to 6.6 g. For each mass value, measurements were carried out for 100 seconds, and five repetitions were performed. The average real coincidence

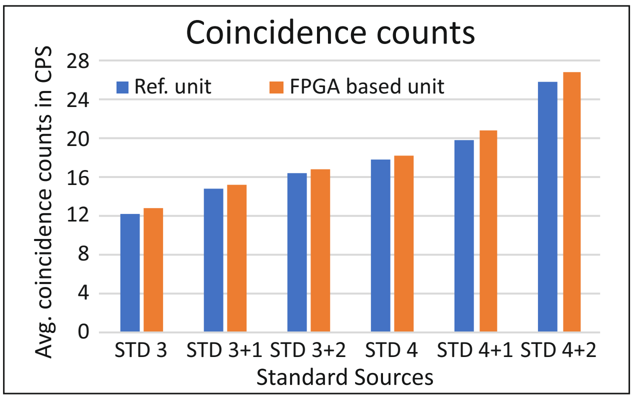


Fig.4: Coincidence counts for Ref. and FPGA based unit with diff. std.

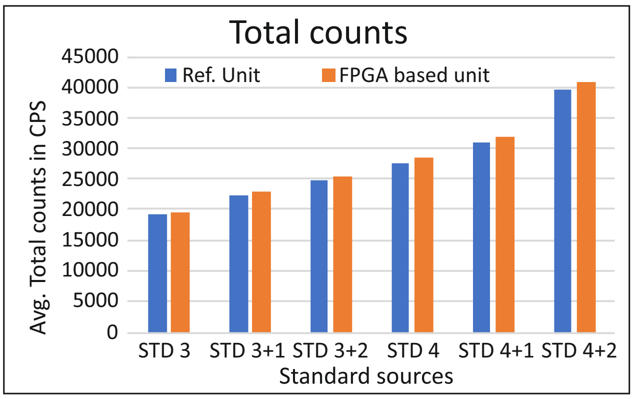


Fig.5: Total counts for Ref. and FPGA based unit with diff. std.

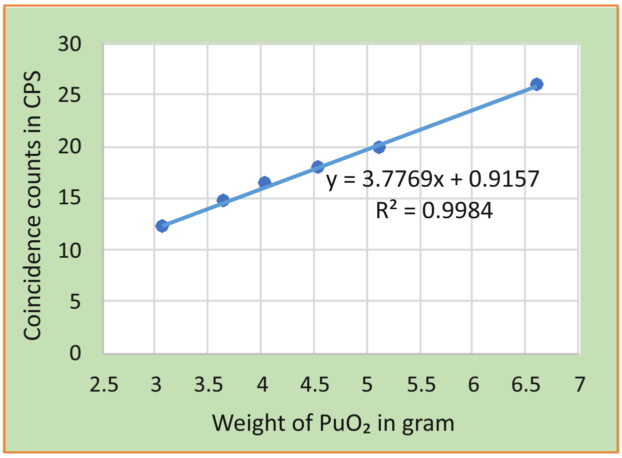


Fig.6: Coincidence counts in CPS Vs PuO_2 Wt. (Ref. unit).

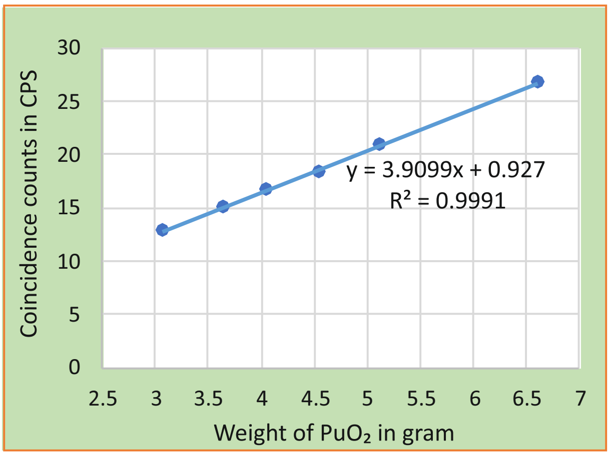


Fig.7: Coincidence counts in CPS Vs PuO_2 Wt. (Ref. unit).

counts and total counts were calculated for both modules. The details are presented in figure 4 and 5.

Figures 6 and 7 show the relationship between source mass and coincidence counts for the reference module and the FPGA-based module, respectively. The linear regression analysis yielded an R^2 value of 0.9984 for the reference module and 0.9991 for the FPGA based module.

Conclusion

This comparative study confirms that discrete IC based coincidence module can be effectively replaced by the proposed FPGA based module. The FPGA implementation offers greater flexibility, allowing parameters such as gate width and pre-delay to be modified through software without hardware changes, making it suitable for future research applications. The obtained R^2 values of 0.9984 for the existing system and 0.9991 for the FPGA based system confirm the good correlation and reliable performance of the developed module.

Future Scope and Possibilities

The FPGA-based design enables modification of well geometry and flexible adjustment of gate width and pre-delay without changing the overall electronic system. This allows optimization of the coincidence window for different detector configurations and sample conditions. The improved timing control enhances discrimination between real and accidental events, resulting in better accuracy. The programmable architecture ensures long-term adaptability.

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