Government of India
Bhabha Atomic Research Centre
Accelerator Control Division

Ref: ACnD/ACSS/RTK/18/93 Date: 29/01/2018

----------TO WHOM SO EVER IT MAY CONCERN----------

Sub: Minor Fabrication job for "Layout design, fabrication, component procurement, mounting and testing of VME64X based general purpose analog I/O & digital I/O cards." conforming to technical specification no ACnD/ACSS/RTK/TS11 dated 24/01/2018

Dear Sir/Madam,

1. Quotations are invited for, "Layout design, fabrication, component procurement, mounting and testing of VME64X based general purpose analog I/O & digital I/O cards" conforming to technical specification no. ACnD/ACSS/RTK/TS11 dated 24/01/2018.
2. Bidder shall quote for purchase of raw materials, fabrication, assembly, integration, testing and supply of all items and its accessories.
3. Taxes and Duties shall be quoted separately.
4. The quotation must reach **The Head, Accelerator Control Division** by 12/02/2018 (12:00 PM) and must be sent in a sealed envelope super scribed with the reference number & the due date given above only through India Ordinary Post/Speed Post.
5. The address on the envelop should read: The Head,
   Accelerator Control Division,
   1-328S, First floor, Modlab-D block,
   BARC, Trombay,
   Mumbai - 400 085.
   (Kind Attn: Shri R T Keshwani, SO/F, ACnD)
6. The bidder shall complete the job within 24 weeks from the date of firm work order issued to the bidder. The finished components shall be delivered by the bidder at Accelerator Control Division, BARC, Trombay, Mumbai - 400 085.
7. Head, Accelerator Control Division reserves the rights to accept / reject any or all quotations without assigning any reason.
8. Delivery charges if any must be clearly mentioned in the offer.
9. Quotation must indicate the validity of offer. Quotation must also indicate the PAN no, GST tax, registration number registered with local ST authority /CST authority. Quotation must be submitted in printed letterhead. Quotations should be preferably neatly typed and corrections are not acceptable. The quotation has to be signed by authorized person with company seal.
10. Drawings / Sketches (if any)must be returned along with the offer.
11. Payment will be made by ECS only after satisfactory completion of work on production of bill, delivery challan and advance stamped receipt. It may be noted that IT@2% shall be deducted from your bills. Also, items intended to be procured/fabricated in this work attract concessional rate of GST as per the said notifications. Exemption Certificate shall be issued on placement of firm PO.
12. Job will be guaranteed against material and manufacturing defects for 1 year from the date of supply.
13. In case of technical clarifications, the suppliers may kindly contact Shri R. T. Keshwani, SO/F, ACnD (Ext No: 022-25593806)

    Encl.: Technical Specification Sheet no: - ACnD/ACSS/RTK/TS11 dated 24/01/2018.

RTKeshwani

29.01.18

Head, ACnD

डॉ. गोपाल जोशी/Dr. Gopal Joshi
अध्यक्ष, त्वरक नियंत्रण प्रभाग/Head, Accelerator Control Division
भारत सरकार/Government of India
भाभा परमाणु अनुसंधान केन्द्र/Bhabha Atomic Research Centre
ट्रॉम्बे, मुंबई/Trombay, Mumbai-400 085.

Specification no.	Revision no.	Date of Issue	No of pages
ACnD/ACSS/RTK/TS11	0	24/01/2018	09

Layout design, fabrication, component procurement, mounting and testing of VME64X based general purpose analog I/O & digital I/O cards.

1.0. Scope of work:

It is required to fabricate, assemble, test and supply VME64x based 6U size electronic boards as per Technical Specifications detailed in annexure II. The job is to be executed as detailed below.

The supplier shall procure all components as per bill of material (BOM in annexure III) enclosed. The layout of PCBs should be designed from schematics provided. PCB's shall assembled with the required components and finally tested for basic functionality before supply. The Front fascia panels to be fabricated and punched as per the details enclosed in annexure II. The indenting authority shall provide all the necessary details required for the job.

2.0. Mode of execution:

a) The final schematic design will be supplied in OrCad Capture format along with the confirmed order. PCB layout files shall be made in cadence allegro format The supplier will have to do fabrication of the PCBs, procurement and mounting of the components as per the final schematic bill of material and testing of the boards.
b) VME carrier board has 14 layers depending on the layout methodology used for routing nets, ground and power supply planes.
c) The supplier shall review the schematic and seek clarifications if required. The part numbers given in BOM in annexure III are indicative only. Any functionally compatible parts can be used with the consent of the indenter.
d) The supplier can suggest any changes to improve the performance of the boards and implement the same with the consent of the indenting officer. The completed layout shall be submitted to the indenting officer for approval if any changes have been incorporated. After the approval, the supplier shall generate the Gerber file in RS-274X format. The supplier has to fabricate the boards from a reputed manufacturer and name of the manufacturer is to be mentioned in the quote.
e) The PCB fabrication process should be carried out as per the following requirements
    - Meeting FCC EC Standard requirements
    - PCB size: 6U (230mm x 160mm) and material FR4 for VME carrier boards with 14 layers.
    - Laser photo plotting technique to be used
    - PCB fabrication with Solder Mask Over Bare Copper (SMOBC) / Hot Air Solder Leveling (HASL) technology and all vias shall be masked.
    - SMD resistor and capacitor of 0402 size
    - Complete Gold flash on full PCB
    - The PCBs should pass all the qualification and Quality control tests including the Bare
      Board with flying Probe Technique
f) Procurement and mounting of the components shall be done as per the bill of material generated from the final schematic.
g) The components shall be assembled and soldered on the PCB as per the conditions explained below. The assembly of the PCB shall be with the following setup:
    - Fully automated SMT setup with pick and place for all standard SMD components during production stage
    - Reflow with forced air convection system
    - Minimum three zones of heating profile with independent reflow zones

- High-resolution microscope visual inspection system.
- ESD safe environment.
- ESD safe soldering station for through-hole components and for wiring.
- The workmanship should be as per the IPC-A-610D electronic assembly standard
- The correct assembling of all the electronic components especially the FPGA (BGA component) shall be ensured.

h) The supplier will fabricate one PCB and populate it as per the design and submit it for testing. During the testing of the board, if any design or manufacturing errors are found, the corrections will be intimated to the supplier. The supplier shall incorporate the changes in the design and layout and will manufacture remaining PCB's and will populate them as per the corrected bill of the material.

i) The front fascia panels for the boards should be fabricated and engraved. They should have good quality standard ejectors suitable for a VME64X chassis. Details of the fascia requirements of carrier boards and mezzanine cards have been explained in annexure II.

j) The supplier shall procure necessary commercial grade components as per the final bill of material generated from OrCad Schematic and assemble them on the board.

k) The supplier will have to demonstrate the basic working of the board like it powers drawing the rated current and none of components showing physical damage or abnormal behaviour.

l) During the testing of the board, if any design or manufacturing error is found, the corrections will be intimated to the supplier. Change in the design will not be major, but may include certain component changes. The supplier shall incorporate the changes in the layout and will manufacture one new board and submit it for testing. The remaining board can be fabricated once this new board is found to be error free. **The supplier will have to supply all the boards as specified in indent in full working condition**

m) Fabrication costs, component cost and testing charges of modules are to be mentioned separately in the quote.

n) Additional charges for correction in layout and Gerber generation should be explicitly mentioned in the quotation for correcting errors in the layout and Gerber files due to errors in the user's schematic files. If the charges are not mentioned, it will be assumed to be "free of charge" and included in the quotation.

o) If the first board is rejected due to manufacturing defects, the supplier will have to supply an additional board as replacement free of cost. **The supplier will have to supply all the boards as specified in indent in full working condition**

p) All the items fabricated shall have onsite warranty for a period of one year from the date of final acceptance against all manufacturing defects.

q) If required the purchaser along with experts will visit the supplier and evaluate the capability of the engineers employed by the supplier. Supplier must give details of jobs undertaken of similar complexity in the past three years for any organization.

r) The supplier must give the details of the infrastructure suitable for this job such as VHDL programming tools, Schematic Capture, PCB layout tools and test equipment such as function generator, Oscilloscopes and logic analyser. In case the firm does not have these tools and equipments but intend to bring them on rent during the execution of the job then it should be clearly mentioned in the technical quotation.

s) The manufacturer shall provide the following documents at the time of supply of the boards:

1. Corrected OrCad Schematic Files
2. Final BOM (Bill of Material).
3. Final PCB layout files in cadence allegro format.
4. Final Gerbers in RS274-X format
5. Pick & Place File
6. N.C. Drill files
7. Drill Drawing (Fabrication Drawing)
8. Layer Stack Report
9. Assembly Diagram (PDF format)
10. Archive of complete design folders including intermediate design files and design documents, datasheets.
11. Well documented codes used for testing of board
12. Detailed operation and testing procedure

3.0 Deliverables:
The following items shall be supplied to ACnD, BARC after satisfactory testing and inspection by indenting authority. The packaging, transportation and safe delivery shall be in scope of supplier.

Sr No	Description	Qty
1	General purpose Analog Input (GPAI) card	05 No.
2	General purpose Analog Output (GPAO) card	05 No.
3	General purpose Digital Input/Output (GPD I/O) card	05 No.

4.0 Documentation Requirements:
4.1 Before commencing manufacturing, supplier shall furnish the following for purchaser's approval:
4.1.1 The fabrication drawing shall be submitted for approval either in soft/ hard copy form.
4.2 The supplier shall submit a quality assurance (QA) plan to the buyer for acceptance. The plan shall ensure that each item offered for acceptance conforms to the requirements herein.

5.0 Requirements of supplier qualification:
5.1 Human resources: The supplier must give the details of human resources including Engineers, Draftsman, assembly mechanic, quality control inspector, etc.

5.2 Infrastructure: The supplier must give the details of infrastructure suitable for this job such as electronic testing equipment, etc. Assembly room and other tools & tackles, Inspection facilities etc.

5.3 Past experience: The supplier must give their past three-year turnover and job executed by them with reference, volume of work and completion schedule, present commitments and anticipated commitments inside and outside India.

5.4 Sub contract: Supplier should list the jobs, which they want to sub-contract. They should also produce the list of sub-contractors and their infrastructures and facilities.

5.5 Supplier shall have necessary electronic hardware test set up at their facility to carry out the above fabrication and testing.

6. 0 Requirement of price and delivery schedule:
6.1 The supplier shall give a lump-sum price with delivery schedule

7.0 Confidentiality clause:
7.1 No party shall disclose any information to any third party concerning the matters under this Contract generally. In particular, any information identified as "Proprietary" in nature by disclosing party shall be kept strictly confidential by the receiving party and shall not be disclosed to any third party without the prior written consent of the original disclosing party. This clause shall apply to sub-contractors, consultants, advisors or the employees engaged by a party with equal force.

7.2 . "Restricted information" categories under section 18 of the Atomic Energy Act, 1962 and "Official secrets" under section 5 of the Official Secrets Act, 1923: Any contravention of the above mentioned provisions by any contractor / sub-contractor, consultant, advisor or the employees of the contractor will invite penal consequences under the aforesaid legislation.

7.3 Prohibition against the use of BARC's name without permission for publicity purpose. The contractor or sub-contractors, consultants, advisors or the employees engaged by a party shall not use BARC's name for publicity purpose through any public media like: press, radio, TV or Internet without any prior approval of BARC (wide circular ref.: 2/Misc- 9/Lgl/2001/92 date 30/04/2001

Annexure II

Technical specifications of general purpose analog & digital I/O cards

The technical specification, interfaces, features and descriptions at block diagram level are detailed below:

1.0 General purpose AI Card:

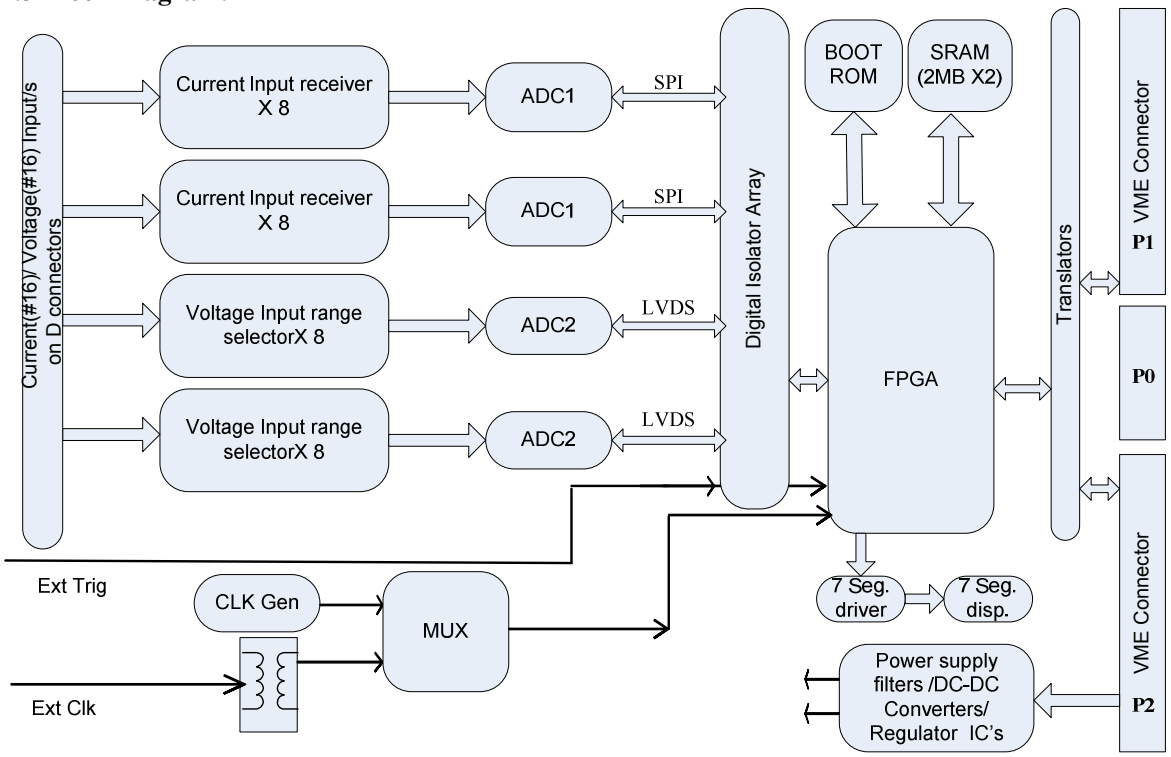
1.1 Features:

1) It has 32 channel analog intputs (AI) out of which 16 AI are current (4-20mA) input. Remaining 16 AI are voltage inputs with selectable input ranges. Each channel has cut of frequency of 100 KHz and has 16 bit resolution.
2) It is VME64X based suitable for 6U height, 160mm depth with front facia, the field interface connector is DB64 type.
3) It is Cyclone IV FPGA based with suitable peripherals for it incorporated.
4) Digital isolators are provided at FPGA signals interfaced to ADC's

1.2 Interfaces:

1) Address lines and data lines of VME64X bus are interfaced to FPGA through translators. FPGA found suitable is Cyclone IV family.
2) From VME connectors 5V, 12V and 3.3V power supplies are used with filters and DC-DC converters to derive voltages suitable for FPGA banks and other digital hardware. FPGA is interfaced to VME bus address and data lines using suitable translators.
3) FPGA shall be interfaced to I2C EPFROM
4) FPGA shall be interfaced to two SRAMs each of 2M capacity.
5) FPGA controls ADC's through SPI via digital isolators.
6) The Digital isolators mentioned in BOM are suitable choice for these SPI lines as they can operate upto 150MHz frequency.
7) The 16 bit 8 channel ADC is used to process current input after this input is passed through a current input receiver.
8) The 16 bit 8 channel ADC of other type is used to process voltage input after this input is passed through a fully differential I/O amplifier which acts as input voltage range selector.
9) Provision to apply external TTL trigger is made available.
10) Either on-board clock generator or external clock is selected using MUX. The o/p of MUX is distributed using clock distributor.
9) 32 channels i/ps are applied at D-type connector.
10) A front facia with suitable markings, and ejector handles shall be used.
11) Each IC has power supply filtering as per its datasheet.

1.3 Block Diagram:

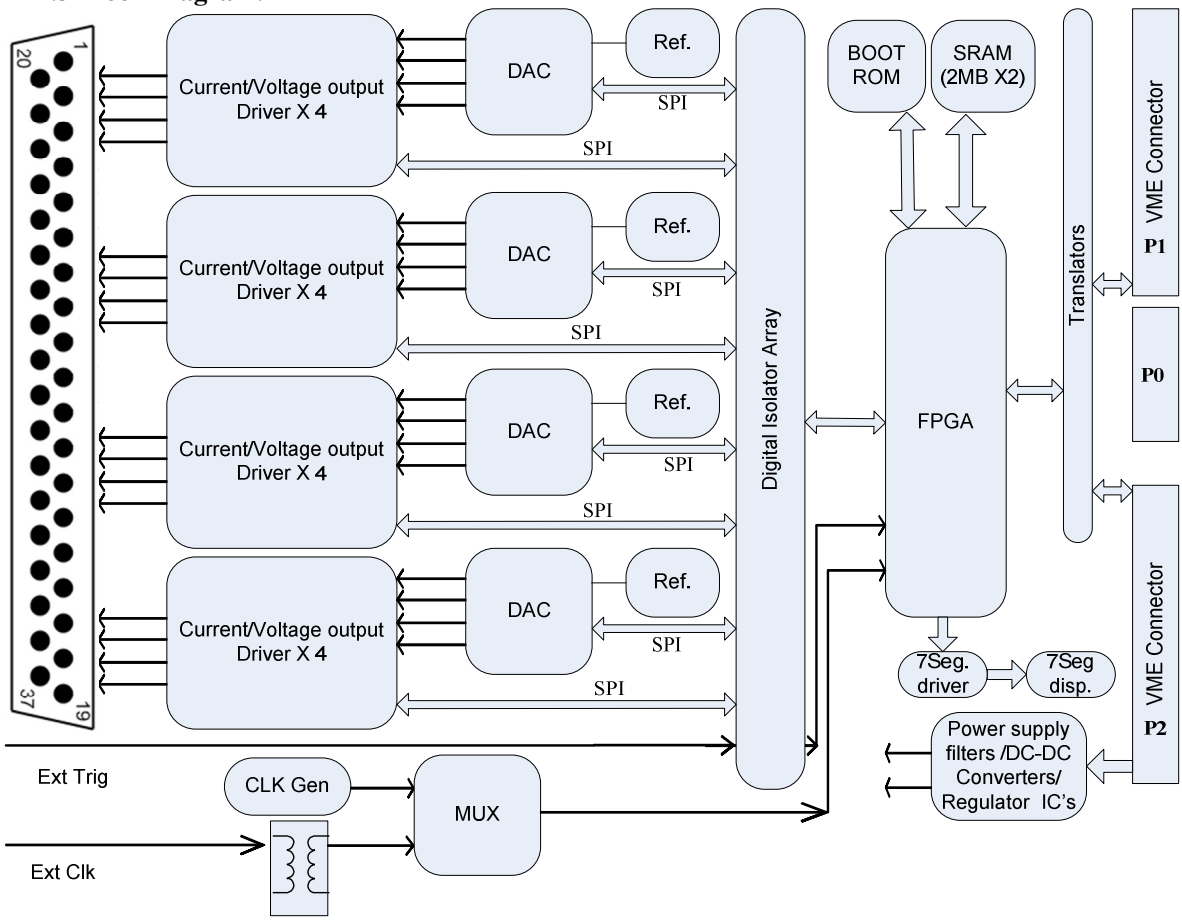


1.4 BOM:
Refer to annexure III for BOM of this card.

2.0 General purpose AO Card:
2.1 Features:
1) It has 16 channel analog output which may be voltage or current (4-20mA) output as programmed. Each channel has cut of frequency of 1MHz and is of 16 bit resolution.
2) It is VME64X based card suitable for 6U height, 160mm depth with front facia, the field interface connector is DB37 type.
3) It is CycloneIV FPGA based with suitable peripherals for it incorporated.
4) Digital isolators are provided at FPGA outputs interfaced to DAC and to current/voltage output driver.

2.2 Interfaces:
1) Address lines and data lines of VME64X bus are interfaced to FPGA through translators. FPGA envisaged suitable is Cyclone IV family.
2) From VME connectors 5V, 12V and 3.3V power supplies are used with filters and DC-DC converters to derive voltages suitable for FPGA banks and other digital hardware. FPGA is interfaced to VME bus address and data lines using suitable translators.
3) FPGA shall be interfaced to I2C EPFROM
4) FPGA shall be interfaced to two SRAMs each of 2M capacity.
5) FPGA controls DAC and output driver through SPI via digital isolators.
6) The Digital isolators mentioned in BOM are suitable choice for these SPI lines as they can operate upto 150MHz frequency.
7) The 16 bit 4 channel DAC is used to produce analog o/p. A high precision OPAMP shall be used to generate reference voltage for each DAC channel.
8) This o/p is applied to Industrial Current/Voltage Output Driverwith Programmable Ranges. This enables producing current or voltage o/p from same card.
9) 16 channels o/ps are finally made available at D-type connector.
10) A front facia with suitable markings, and ejector handles shall be used.
11) Each IC has power supply filtering as per its datasheet.

2.3 Block Diagram:



2.4 BOM: Refer to annexure III for BOM of this card.

3.0 General purpose digital I/O Card:

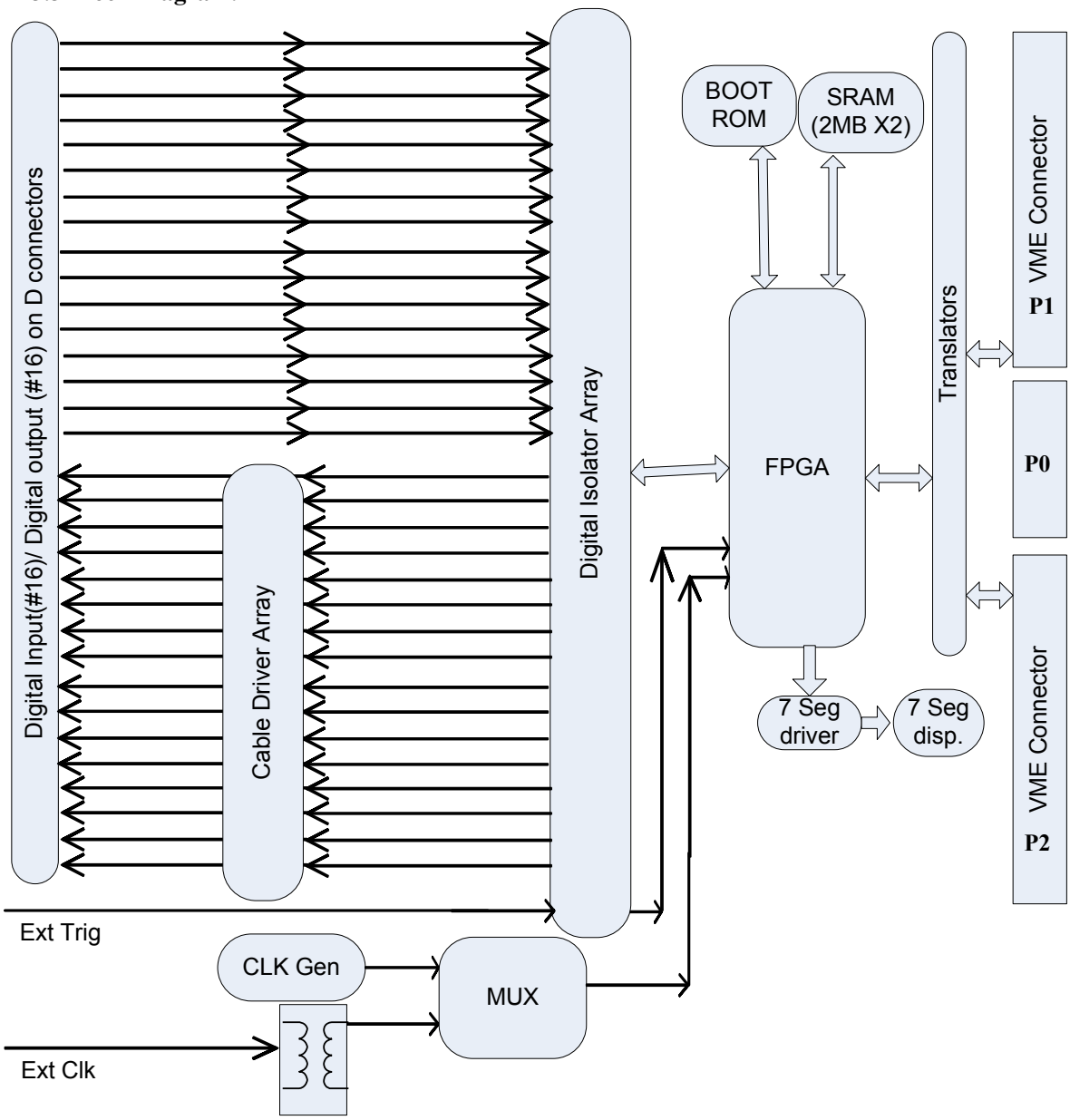
3.1 Features:

1) It has 16 digital TTL inputs
2) It has 16 digital outputs with 50 ohm driving capability.
3) It is VME64X based suitable for 6U height, 160mm depth with front facia, and the field interface connector is DB64 type.
3) It is Cyclone IV FPGA based with suitable peripherals for it incorporated.
4) Digital isolators are provided at FPGA outputs interfaced to I/o hardware.

3.2 Interfaces:

1) Address lines and data lines of VME64X bus are interfaced to FPGA through translators. FPGA envisaged suitable is Cyclone IV family Altera make.
2) From VME connectors 5V, 12V and 3.3V power supplies are used with filters and DC-DC converters to
derive voltages suitable for FPGA banks and other digital hardware. FPGA is interfaced to VME bus address and data lines using suitable translators.
3) FPGA shall be interfaced to I2C EPFROM
4) FPGA shall be interfaced to two SRAMs each of 2M capacity.
5) FPGA controls digital outputs and generates digital inputs via digital isolators.
6) The Digital isolators mentioned in BOM are suitable choice as they can operate upto 150MHz frequency.
7) 32 I/O channels are finally made available at D-type connector.
8) A front facia with suitable markings, and ejector handles shall be used.
9) Each IC has power supply filtering as per its datasheet.

3.3 Block Diagram:



3.4 BOM: Refer to annexure III for BOM of this card.

Annexure III
Bill of material

The part numbers given in the BOM are indicative only. Any functionally compatible parts can be used with the consent of the indenter.

Bill of Material for One AI card
Total No of boards required 05 nos

Sr No	Item name	Part no.	Qty
1	FPGA	Cyclone IV EP4CE115F29C8N	01 no
2	I2C EPROM	EPCS128	01 no
3	SRAM (2M)	CY62177EV30	02 no
4	Digital isolators	ADUM160E	04 nos
5	Digital isolators	ADUM7642	02 nos
6	Digital isolators	ADN4650	04 nos.
7	Digital isolators	ADN4651	02 nos.
8	ADC1	AD7606	02 nos
9	ADC2	LT2329-16	02 nos.
10	DI/DO OPAMP	AD5750BCPZ	16 nos
11	DC-DC converter	RPA20-2412DAW	01 no
12	Current receiver	RCV420	16 no
13	Mux	LMK04906	01 no.
14	Translators	SN74VMEH22501A	
15	D type connector	64 pin female	01 nos.
16	Front facia with ejector handles.	-	01 no.
17	Seven segment with driver	MAX6952EAX, TA07-11CGKWA	01 no.
18	VME P0, P1 and P2 connectors	As per VME64X standard	01 set
19	Clock generator	MC2016K25	01 no.
20	Transformer	ADTT1-1+	01 no.
21	LDO regulator	LT3015	01 no.
22	LDO regulator	LT1086	02 no.

Bill of Material for One AO card
Total No of boards required 05 nos

Sr No	Item name	Part no.	Qty
1	FPGA	Cyclone IV EP4CE115F29C8N	01 no
2	I2C EPROM	EPCS128	01 no
3	SRAM (2M)	CY62177EV30	02 no
4	Digital isolators	ADUM160E	06 nos
5	Digital isolators	ADUM161E	04 nos
6	DAC	DAC8814ICDBT	04 nos
7	High precision OPAMPs	OPA4277	16 nos.
8	Current/Voltage Output Driver	AD5750BCPZ	16 nos
9	DC-DC converter	RPA20-2412DAW	01 no
10	Translators	SN74VMEH22501A	10 no.
11	D type connector	37 pin female	01 nos.
12	Front facia with	-	01 no.

	ejector handles.		
13	Seven segment with driver	MAX6952EAX, TA07-11CGKWA	01 no.
14	VME P0, P1 and P2 connectors	As per VME64X standard	01 set
15	Mux	LMK04906	01 no.
16	Clock generator	MC2016K25	01 no.
17	Transformer	ADTT1-1+	01 no.
18	LDO regulator	LT3015	01 no.
19	LDO regulator	LT1086	02 no.

Bill of Material for One Digital I/O card
Total No of boards required 05 nos

Sr No	Item name	Part no.	Qty
1	FPGA	Cyclone IV EP4CE115F29C8N	01 no
2	I2C EPROM	EPCS128	01 no
3	SRAM (2M)	CY62177EV30	02 no
4	Digital isolators	ADUM160N	12 nos
5	Cable drivers	SN64BCT25245DW	02 nos
7	DC-DC converter	RPA20-2405SAW	01 no
9	Translators	SN74VMEH22501A	
10	D type connector	64 pin female	01 nos.
11	Front facia with ejector handles.	-	01 no.
12	Seven segment with driver	MAX6952EAX, TA07-11CGKWA	01 no.
13	VME P0, P1 and P2 connectors	As per VME64X standard	01 set
14	Mux	LMK04906	01 no.
15	Clock generator	MC2016K25	01 no.
16	Transformer	ADTT1-1+	01 no.